

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**

Attorney Docket No.
2885/96

Serial No.
10/551,891

Applicant(s)
VORBACH

Filing Date
August 28, 2006

Group Art Unit
2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,571,736	February 18, 1986	Agrawal et al.			
	5,477,525	December 19, 1995	Masanobu Okabe			
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	6,426,649	July 30, 2002	Fu et al.			
	6,483,343	November 19, 2002	Faith et al.			
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FOREIGN PATENT DOCUMENTS

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						YES	NO
	2001-167066	June 22, 2001	Japan			Abstract	
	11-184718	July 9, 1999	Japan			Abstract	
	5-265705	October 15, 1993	Japan			Abstract	

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	Altera, "APEX 20K Programmable Logic Device Family," Altera Corporation Data Sheet, March 2004, ver. 5.1, pp. 1-117.
	Chaudhry, G.M. et al., "Separated caches and buses for multiprocessor system," Circuits and Systems, 1993; Proceedings of the 36 th Midwest Symposium on Detroit, MI, USA, 16-18 August 1993, New York, NY IEEE, 16 August 1993, Pages 1113-1116, XP010119918 ISBN: 0-7803-1760-2.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Pages 434-437, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
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	Jantsch, Axel et al., "Hardware/Software Partitioning and Minimizing Memory Interface Traffic," Electronic System Design Laboratory, Royal Institute of Technology, ESDLab, Electrum 229, S-16440 Kista, Sweden (April 1994), pp. 226-231.
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EXAMINER	/Keith Vicary/
	DATE CONSIDERED 03/23/2010
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	